WHAT IS CLAIMED IS:

1. A voltage controlled oscillator comprising:

a first VCO element having an output;

a second VCO element having an input and an output, the input coupled to the output of the first VCO element;

a first gated circuit having an input and an output, the input coupled to the output of the first VCO element;

a second gated circuit having an input and an output, the input coupled to the output of the second VCO element; and

a first logic circuit configured to receive a VCO enable signal, the output of the first VCO element, and the output of the second VCO element, and further configured to provide a first output enable signal to the first gated circuit and a second output enable signal to the second gated circuit.

2. The voltage controlled oscillator of claim 1 wherein the first logic circuit retimes the VCO enable signal with a signal at the output of the first VCO element to provide the first output enable signal.

3. The voltage controlled oscillator of claim 2 wherein the first logic circuit retimes the VCO enable signal using a register.

4. The voltage controlled oscillator of claim 2 wherein the first logic circuit retimes the first output enable signal with a signal at the output of the second VCO element to provide the second output enable signal.

5. The voltage controlled oscillator of claim 4 wherein the first logic circuit retimes the first output enable signal using a register.

6. The voltage controlled oscillator of claim 5 wherein the first logic circuit retimes the first output enable signal using a latch.

7. The voltage controlled oscillator of claim 2 wherein the output of the first gated circuit couples to a first counter and the output of the second gated circuit coupled to the second gated counter.

8. The voltage controlled oscillator of claim 2 wherein the first VCO element and the second VCO element form a portion of a ring oscillator.

9. The voltage controlled oscillator of claim 2 wherein the output of the first VCO element is buffered by a first buffer and the output of the second VCO element is buffered by a second buffer.

10. The voltage controlled oscillator of claim 2 wherein the voltage controlled oscillator is formed on an integrated circuit.

11. The voltage controlled oscillator of claim 10 wherein the VCO enable signal is generated following an increase in a supply voltage for the integrated circuit.

12. The voltage controlled oscillator of claim 2 wherein the VCO enable signal is a reset signal that resets a counter.

13. A method of enabling outputs of a voltage controlled oscillator comprising:

receiving a VCO enable signal;

receiving a first VCO output signal;

receiving a second VCO output signal, the second VCO output signal phase shifted from the first VCO output signal; and

retiming the VCO enable signal with the first VCO output signal to generate a first VCO output enable signal.

14. The method of claim 13 further comprising:

retiming the first VCO output enable signal with the second VCO output signal to generate a second VCO output enable signal.

15. The method of claim 13 wherein when the first VCO output enable signal is asserted, the first VCO output signal is received by a logic circuit.

16. The method of claim 15 wherein the logic circuit is a counter.

17. The method of claim 15 wherein the logic circuit is a first-in-first-out memory.

18. A voltage controlled oscillator comprising:

means for generating a plurality of clock outputs including a first clock output and a second clock output, the first and second clock outputs shifted in phase relative to each other;

means for gating the first clock output and the second clock output;

means for receiving a VCO enable signal; and

means for retiming the VCO enable signal to the first clock output to generate a first gating signal,

wherein the first gating signal controls the means for gating the first clock output.

19. The voltage controlled oscillator of claim 18 further comprising:

means for retiming the first gating signal using the second clock output to generate a second gating signal,

wherein the second gating signal controls the means for gating the second clock output.

20. The voltage controlled oscillator of claim 19 further comprising:

means for counting pulses of the gated first clock output to generate a first counter output.